What is claimed is:

1. An addition circuit for producing a sum of four redundant binary numbers, wherein each number includes an operand field and a sparse carry-save field, comprising:

a 4:2 compression adder for receiving each of the operand fields of the four redundant binary numbers, and producing a first sum field and a first carry field therefrom;

a 4:3 compression adder for receiving each of the sparse carry-save fields of the four redundant binary numbers, and producing a second sum field therefrom;

a 3:2 compression adder for receiving the first sum field, the first carry field and the second sum field, and producing a third sum field and a second carry field therefrom;

wherein the third sum field and the second carry field are the sum of the four redundant binary numbers.

2. An addition circuit according to claim 1, wherein the 4:2 compression adder includes a cascade of a first full adder and a second full adder.

3. An addition circuit according to claim 1, wherein the 4:3 compression adder includes a binary summer for receiving four input bits of equal weight, and producing a three bit binary output word representative of the sum of the four input bits.

4. An addition circuit according to claim 1, wherein the 3:2 compression adder includes a full adder.

5. An addition circuit according to claim 1, wherein the 4:3 compression adder distributes bits within the second sum field so as to correspond to the significance of the sparse carry-save field.

6. An addition circuit according to claim 1, wherein each of the four redundant binary numbers is in radix-16 format, so as to include a sparse carry-save bit for every four operand bits.

7. An addition circuit for producing a sum of four redundant binary numbers, wherein each number includes an operand field and a sparse carry-save field, comprising:

means for receiving each of the operand fields of the four redundant binary numbers, and producing a first sum field and a first carry field therefrom;

means for receiving each of the sparse carry-save fields of the four redundant binary numbers, and producing a second sum field therefrom;

means for receiving the first sum field, the first carry field and the second sum field, and producing a third sum field and a second carry field therefrom;

wherein the third sum field and the second carry field are the sum of the four redundant binary numbers.

8. An addition circuit according to claim 7, wherein the means for receiving each of the operand fields includes a cascade of a first full adder and a second full adder.

9. An addition circuit according to claim 7, wherein the means for receiving each of the carry-save fields includes a binary summer for receiving four input bits of equal weight, and producing a three bit binary output word representative of the sum of the four input bits.

10. An addition circuit according to claim 7, wherein the means for receiving the first sum field, the first carry field and the second sum field includes a full adder.

11. An addition circuit according to claim 7, wherein the means for receiving each of the carry-save fields distributes the second sum field so as to correspond to the significance of the sparse carry-save field.

12. An addition circuit according to claim 7, wherein each of the four redundant binary numbers is in radix-16 format, so as to include a sparse carry-save bit for every four operand bits.

13. A method of producing a sum of four redundant binary numbers, wherein each number includes an operand field and a sparse carry-save field, comprising:

receiving each of the operand fields of the four redundant binary numbers, and producing a first sum field and a first carry field therefrom;

receiving each of the carry-save fields of the four redundant binary numbers, and producing a second sum field therefrom;

receiving the first sum field, the first carry field and the second sum field, and producing a third sum field and a second carry field therefrom;

wherein the third sum field and the second carry field are the sum of the four redundant binary numbers.

14. A method according to claim 13, further including using a 4:2 compression adder to produce the first sum field and the first carry field.

15. A method according to claim 13, further including using a 4:3 compression adder to produce the second sum field.

16. A method according to claim 13, further including using a 3:2 compression adder to produce the third sum field and the second carry field.

17. A method according to claim 13, further including distributing bits within the second sum field so as to correspond to the significance of bits within the sparse carry-save field.

18. An addition circuit for producing a sum of four redundant binary numbers, wherein each number includes an operand field and a sparse carry-save field, comprising:

a 4:2 compression adder, including a cascade of a first full adder and a second full adder, for receiving each of the operand fields of the four redundant binary numbers, and producing a first sum field and a first carry field therefrom;

a 4:3 compression adder, including a binary summer for receiving four input bits of equal weight and producing a three bit binary output word representative of the sum of the four input bits, for receiving each of the carry-save fields of the four redundant binary numbers, and producing a second sum field therefrom;

a 3:2 compression adder, including a full adder, for receiving the first sum field, the first carry field and the second sum field, and producing a third sum field and a second carry field therefrom;

wherein the third sum field and the second carry field are the sum of the four redundant binary numbers.

19. A method of producing a sum of four redundant binary numbers, wherein each number includes an operand field and a sparse carry-save field, comprising:

receiving each of the operand fields of the four redundant binary numbers, and producing, via a 4:2 compression adder, a first sum field and a first carry field therefrom;

receiving each of the carry-save fields of the four redundant binary numbers, and producing, via a 4:3 compression adder, a second sum field therefrom;

receiving the first sum field, the first carry field and the second sum field, and producing, via a 3:2 compression adder a third sum field and a second carry field therefrom;

wherein the third sum field and the second carry field are the sum of the four redundant binary numbers.

20. A method of producing a sum of at least two redundant binary numbers, wherein each number includes an operand field and a sparse carry-save field, comprising:

receiving each of the operand fields of the at least two redundant binary numbers, and producing a first sum field and a first carry field therefrom;

receiving each of the sparse carry-save fields of the four redundant binary numbers, and producing a second sum field therefrom, wherein a distribution of bits within the second sum field corresponds to a sparse distribution within the sparse carry-save fields;

receiving the first sum field, the first carry field and the second sum field, and producing a third sum field and a second carry field therefrom;

wherein the third sum field and the second carry field are the sum of the four redundant binary numbers.